FIG. 1

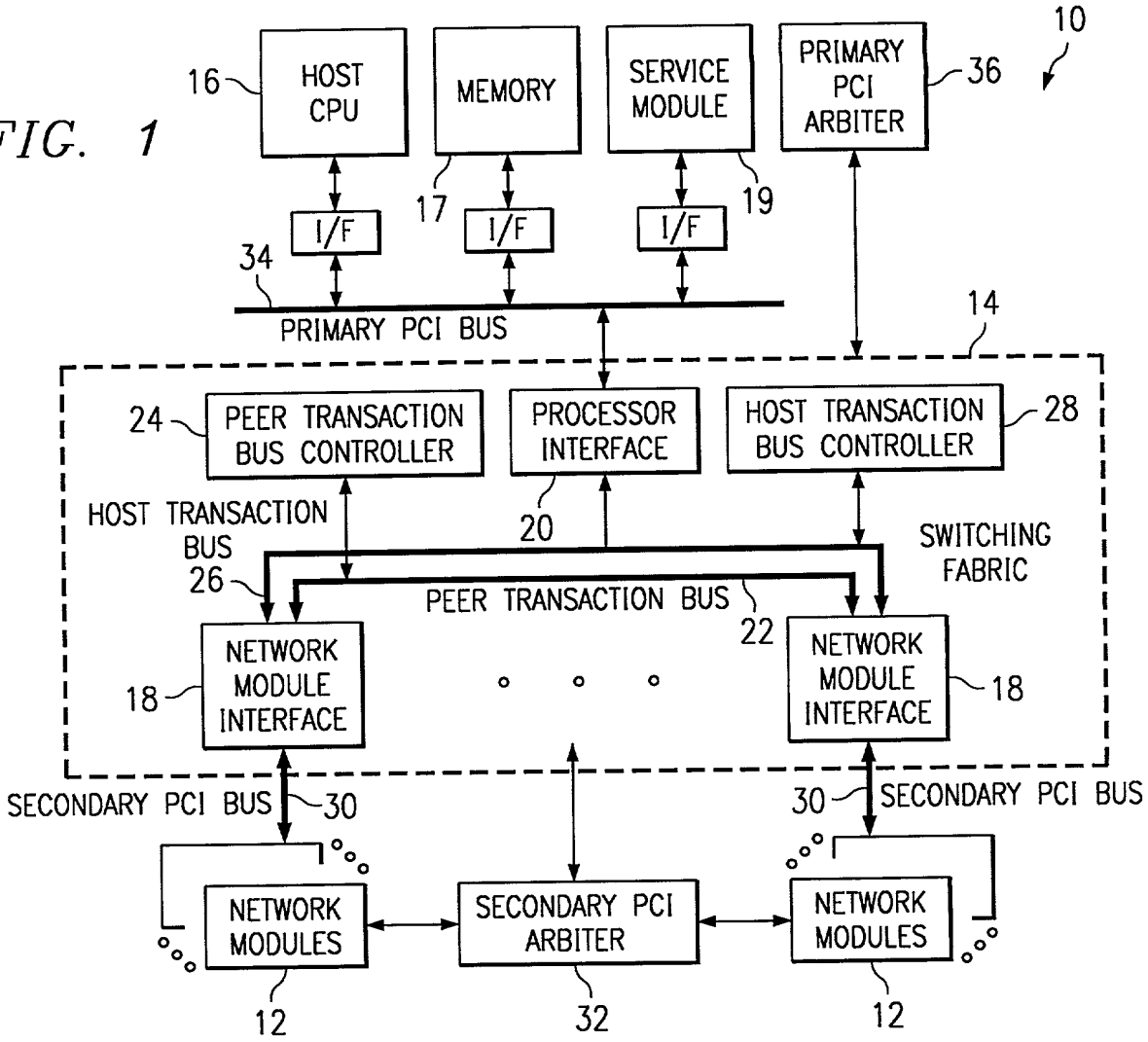
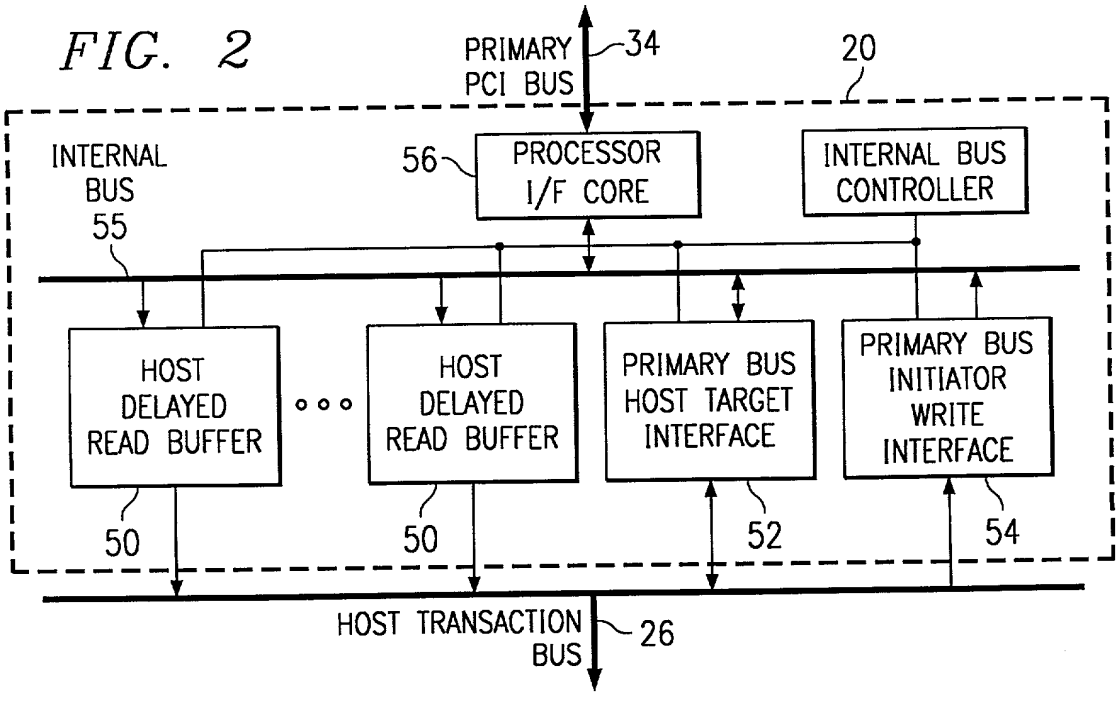

10
16
HOST CPU
MEMORY
SERVICE MODULE
PRIMARY PCI ARBITER
36
17
19
I/F
I/F
I/F
34
PRIMARY PCI BUS
14
24
PEER TRANSACTION BUS CONTROLLER
PROCESSOR INTERFACE
HOST TRANSACTION BUS CONTROLLER
28
20
HOST TRANSACTION BUS
26
SWITCHING FABRIC
PEER TRANSACTION BUS
22
NETWORK MODULE INTERFACE
18
NETWORK MODULE INTERFACE
18
SECONDARY PCI BUS
30
30
SECONDARY PCI BUS
NETWORK MODULES
SECONDARY PCI ARBITER
NETWORK MODULES
12
32
12

FIG. 2


PRIMARY PCI BUS
34
20
INTERNAL BUS 55
56
PROCESSOR I/F CORE
INTERNAL BUS CONTROLLER
HOST DELAYED READ BUFFER
HOST DELAYED READ BUFFER
PRIMARY BUS HOST TARGET INTERFACE
PRIMARY BUS INITIATOR WRITE INTERFACE
50
50
52
54
HOST TRANSACTION BUS
26

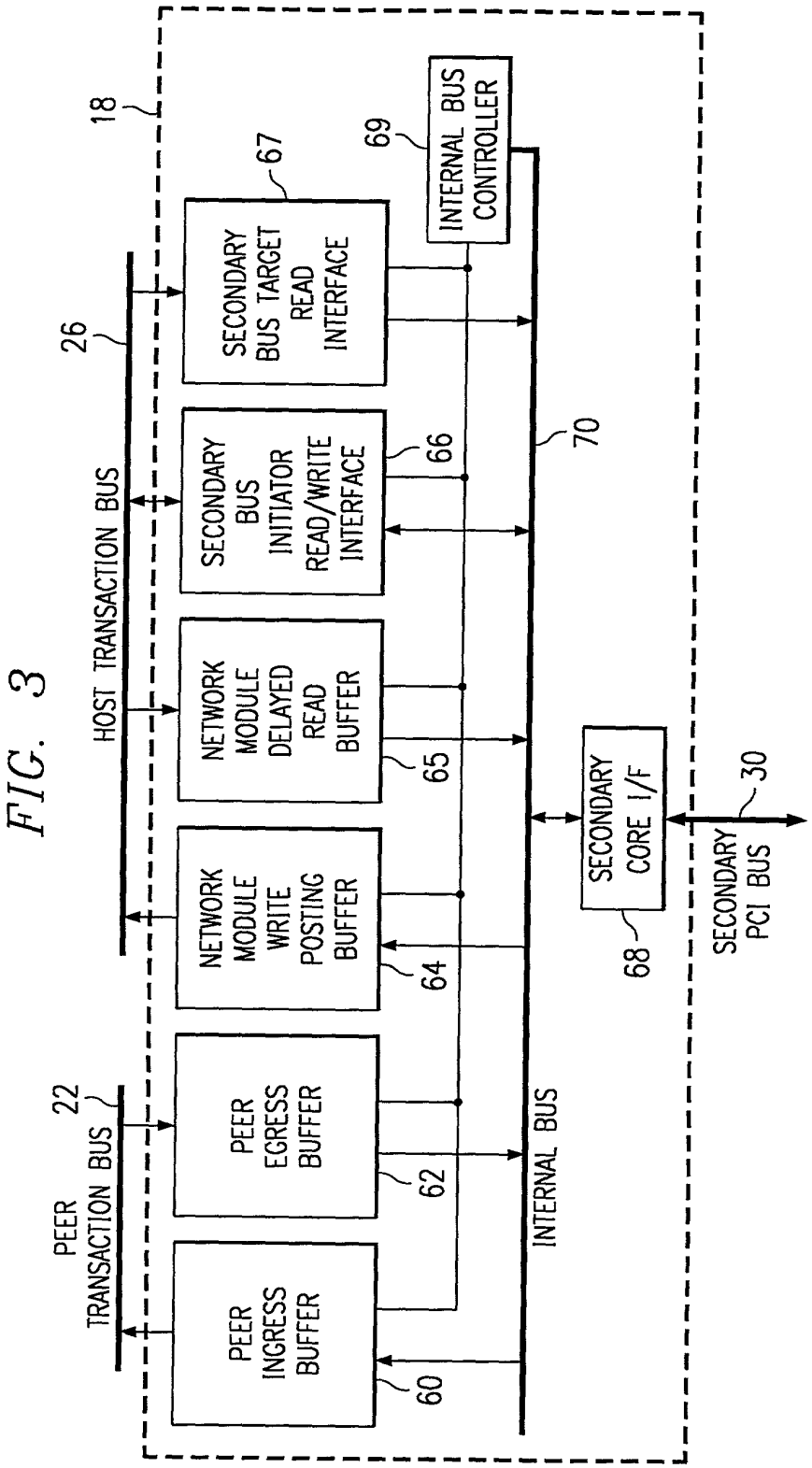
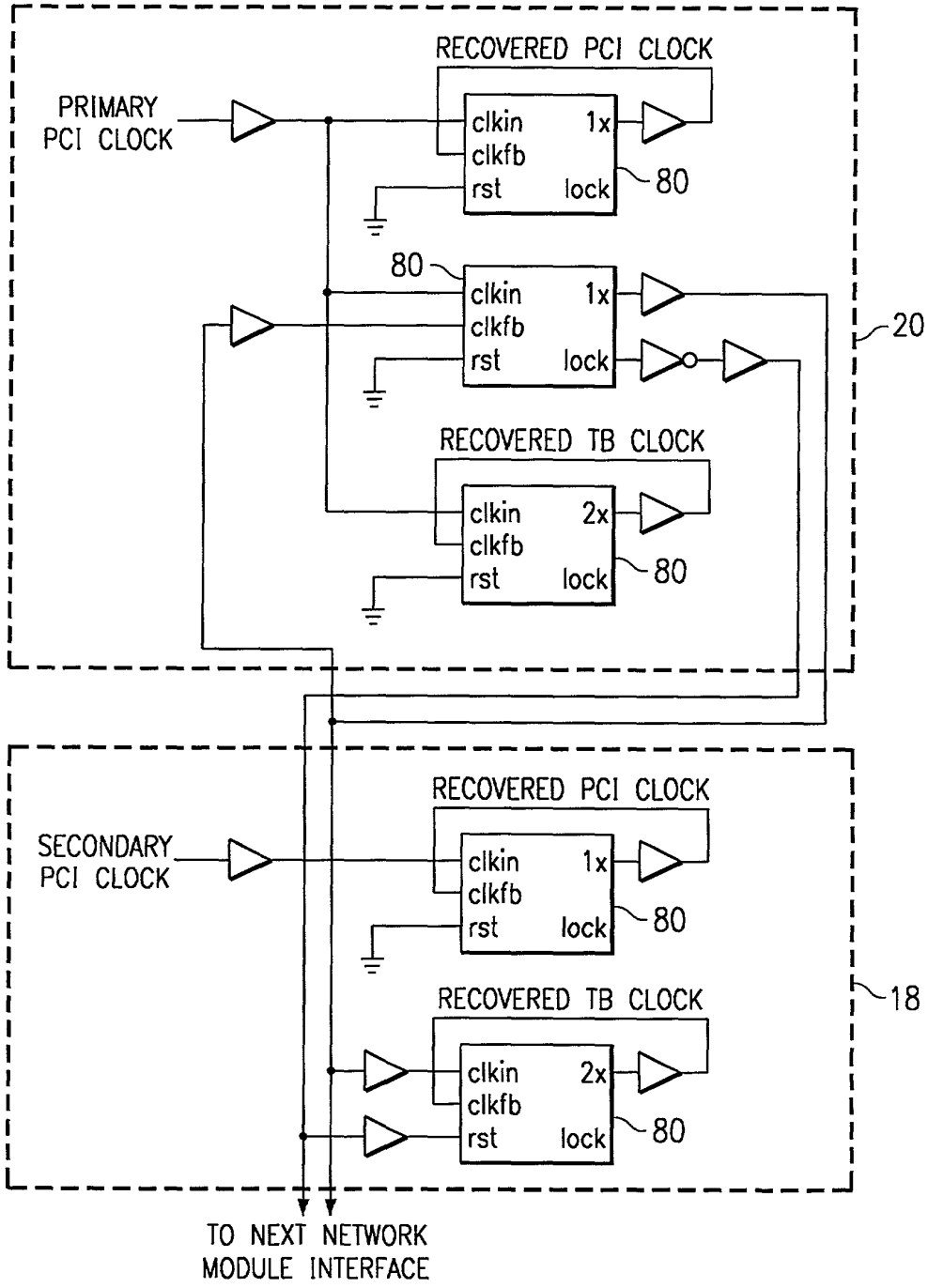

18
HOST TRANSACTION BUS
26
PEER TRANSACTION BUS
22
PEER INGRESS BUFFER
60
PEER EGRESS BUFFER
62
NETWORK MODULE WRITE POSTING BUFFER
64
NETWORK MODULE DELAYED READ BUFFER
65
SECONDARY BUS INITIATOR READ/WRITE INTERFACE
66
SECONDARY BUS TARGET READ INTERFACE
67
INTERNAL BUS CONTROLLER
69
INTERNAL BUS
70
SECONDARY CORE I/F
68
SECONDARY PCI BUS
30

FIG. 3

FIG. 4


RECOVERED PCI CLOCK
PRIMARY PCI CLOCK
clkin
clkfb
rst
1x
lock
80
RECOVERED TB CLOCK
2x
20
SECONDARY PCI CLOCK
18
TO NEXT NETWORK MODULE INTERFACE